Frame Deep Down Set - Large Die Pad
Package PSSO16
Technology VIPower M0L7

Revision history			
Rev.	**Date of Release**	**Author**	**Changes description**
1.0	November 6th 2017	A.Vilardo - ADG Reliability Catania	Creation

Table of contents

Section	Pag	Content
1	3	Reliability evaluations overview
1.1	3	Objectives
1.2	4	Results
2	5	Traceability
3	6	Devices characteristics
3.1	6	Generalities
3.2	7	Pins connection
3.3	7	Blocks diagram
3.4	7	Bonding diagram
4	8	Reliability qualification plan and results – Summary table
5	13	Robustness validation activity results

- 1. Reliability evaluations overview

1.1 Objectives

The Deep Down Set frame in the so called ***"standard die pad"*** for package PSSO16 involving the VIPower products designed in M0L7 Technology was qualified both for Shenzhen (SHZ-China) and Bouskoura (BSK-Morocco) assembly plants (ST reference reports # RR000215CT2235 for SHZ and RR001613CT2235 for BSK).

The so called ***"large die pad"*** frame differs from the ***"standard die pad"*** one only for dimension while no change occurs in the material:

- Standard die pad dimension: 2.49 x 3.21mm
- Large die pad dimension: 2.49 x 3.61mm.

Aim of this report is to present the results of the reliability evaluations performed on **VN7016AJ-E** (XV08 as ST internal silicon line) chosen as test vehicle to qualify those frame dimension change.

This is a single channel High-side driver with Multi Sense analog feedback product for Automotive Applications designed in VIPower M0L7 technology.

The qualification was done according to **AEC_Q100 Rev.H** specification following the path described here below:

Test group as per **AEC-Q100 Rev.G**		Performed (Y/N)	Comment
A	Accelerated Environment Stress	Y	
B	Accelerated Lifetime Simulation	N	Not required for this change
C	Package Assembly Integrity	Y	
D	Die Fabrication Reliability	N	Not required for this change
E	Electrical Verification	Y	
F	Defect Screening	N	To be implemented starting from first production lot
G	Cavity Package Integrity	N	Not applicable

See details per each test group in section 4 of this report.

In the below table a comparison between the AEC-Q100 and ZVEI requirements vs the applied ST qualification plan is reported:

	Test Group A					Test Group B		Test Group C				Test Group D					Test Group E					
	THB	AC	TC	PTC	HTSL	HTOL	ELFR	WBS	WBP	SD	PD	EM	TDDB	HCI	NBTI	SM	HBM	CDM	LU	ED	EMC	SC
AEC-Q100		x	x	x						x	x											x
ZVEI		x	x	x						x	x											x
ST		x	x	x				x	x	x	x											x

No deviation between AEC-Q100 / ZVEI requirements and ST qualification plan

1.2 Results

All reliability tests have been completed with positive results neither functional nor parametric rejects were detected at final electrical testing.

A robustness validation activity (2x AEC-Q100 requirement) was also completed with positive results, see details in section 5 of this report.

The Short Circuit Characterization is not yet started.

Based on the overall positive results we consider the products qualified from a reliability point of view.

- 2. Traceability

Wafer fab information	
Wafer fab manufacturing location	ST CT8 Catania (Italy) and ST SG8 Singapore
Wafer diameter (inches)	8
Silicon process technology	VIPower M0L7
Die finishing back side	Ti-Ni-Au
Die size (micron)	2800x1930
Metal levels / materials	2 levels / Ti/TiN/Ti/AlCu/TiN (3.18 µm last level)
Die finishing front side	Teos + PTeos + SiOn + PIX

Assembly Information	
Assembly plant location	ST Shenzhen (China) and ST Bouskoura (Morocco)
Package description	PowerSSO16
Molding compound	RESIN SUMITOMO EME-G700LS D14mm W4.4g
Wires bonding materials/diameters	Cu 1.2mils (on input) / Cu 2.5mils (on output)
Die attach material	PREFORM Pb/Ag/Sn 95.5/2.5/2 D.50mm SSD

Qualification lots Information for Shenzhen		
	Diffusion Lots #	**Assembly Lots #**
Lot 1	C551F17	GK71015K01
Lot 2	5638JC2	GK71015J01
Lot 3	5638K1J	GK71015H01

Qualification lots Information Bouskoura		
	Diffusion Lots #	**Assembly Lots #**
Lot 1	5529X0R	CZ64403X02
Lot 2	Y241585	CZ6440GD01
Lot 3	C551F17	CZ64407002

Reliability Information	
Reliability test execution location	ST Catania (Italy)

- 3. Devices characteristics

3.1 Generalities

life.augmented

VN7016AJ-E

High-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data

PowerSSO-16

GAPGCFT00327

Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	16 mΩ
Current limitation (typ)	I_{LIMH}	77 A
Stand-by current (max)	I_{STBY}	0.5 µA

- General
  - Single channel smart high side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/ disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery with external components
  - Electrostatic discharge protection

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Headlamps

Description

The VN7016AJ-E is a single channel high-side driver manufactured using ST proprietary VIPower® technology and housed in PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

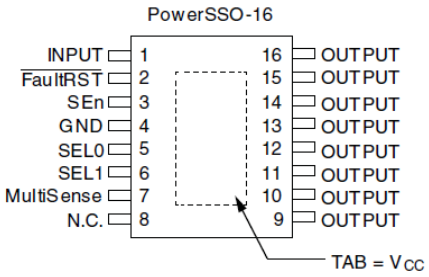
The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

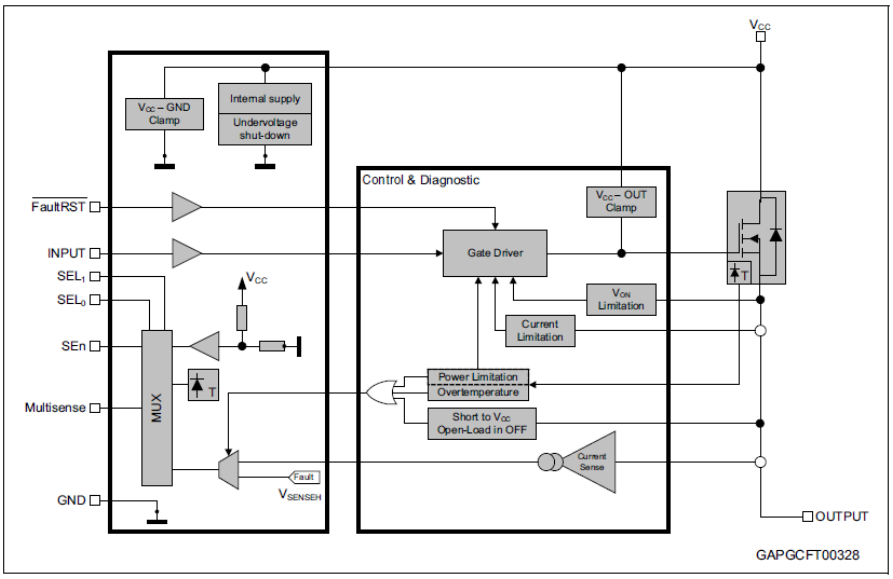
A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

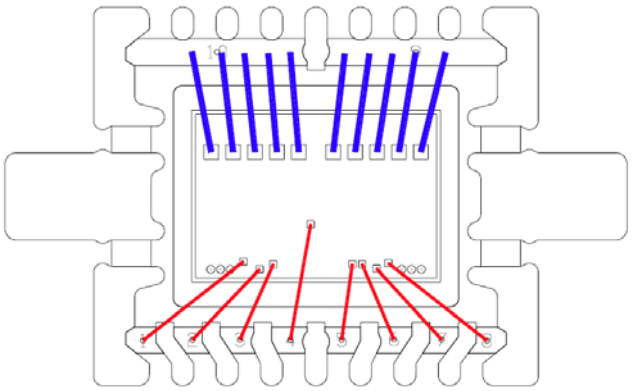
3.2 Pins connection



3.3 Blocks diagram



3.4 Bonding diagram



- 4. Reliability qualification plan and results

Test group A: Accelerated Environment Stress					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
A1	**PC** Pre Cond	- Preconditioning according to Jedec JESD22-A113F including 5 Temperature Cycling Ta=-40ºC/+60ºC - Reflow according to level 3 Jedec JSTD020D-1 - 100 Temperature Cycling Ta=-50ºC/+150ºC	Before AC, TC, PTC. Reliability executed on units soldered on PCB		
A2	**THB** Temp Humidity Bias	Ta=85ºC, RH=85%, Vcc=24V for 1000 hours	-	-	Not required for this change
A3	**AC** Autoclave	**ENV. SEQ.** Environmental Sequence **TC** (Ta=-65ºC / +150ºC for 100 cycles) + **AC** (Ta=121ºC, Pa=2atm for 96 hours)	77/6	0/77/6	
A4	**TC** Temp. Cycling	Ta=-65ºC / +150ºC for 500 cycles	77/6	0/77/6	
A5	**PTC** Power Temp. Cycling	Ta=-40ºC / +125ºC for 1000 cycles.	45/1	0/45/1	Incandescent lamps as loads - H4/65W - ton=10ms, toff=30s, - 120K activations within 1000cy
A6	**HTSL** High Temp. Storage Life	Ta=150ºC for 1000 hours.	-	-	Not required for this change

Test group B: Accelerated Lifetime Simulation					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
B1	**HTOL** High Temp. Op. Life	Bias Dynamic stress (JESD22-A108) Tj=150ºC for 1000 hours	-	-	Not required for this change
B2	**ELFR** Early Life Failure Rate	Parts submitted to **HTOL** per JESD22-A108 requirements; GRADE 1: 24 hours at 150ºC	-	-	Not required for this change
B3	**EDR** Endurance Data Retention	Only for memory devices	-	-	Not Applicable

Test group C: Package Assembly Integrity					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
C1	**WBS** Wire Bond Shear		30 bonds /minimum 5 units/6 lot	All measurement within spec limits	
C2	**WBP** Wire Bond Pull		30 bonds /minimum 5 units/6 lot	All measurement within spec limits	
C3	**SD** Solderability		15/6	All measurement within spec limits	
C4	**PD** Physical Dimensions		10/6	All measurement within spec limits	
C5	**SBS** Solder Ball Shear	Only for BGA package	-	-	Not Applicable
C6	**LI** Lead Integrity	Not required for Surface Mount Devices	-	-	Not Applicable

Test group D: Die Fabrication Reliability					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
D1	**EM** Electromigration		Not required for this change		
D2	**TDDB** Time Dependent Dielectric Breakdown				
D3	**HCI** Hot Carrier Injection				
D4	**NBTI** Negative Bias Temperature Instability				
D5	**SM** Stress Migration				

Test group E: Electrical Verification					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
E2	**ESD** HBM / MM		-	-	Not required for this change
E3	**ESD** CDM		-	-	Not required for this change
E4	**LU** Latch-Up		-	-	Not required for this change
E5	**ED** Electrical Distributions	Performed by data comparison on production parts between old and new assembly plants Testing temperature based on std production flow	-	-	Not required for this change
E7	**CHAR** Characterization		-	-	Not Applicable
E9	**EMC** Electromagnetic Compatibility		-	-	Not required for this change
E10	**SC** Short Circuit Characterization	According to **AEC-Q100-012**	10/6	To be performed	

Test group F: Defects Screening Tests					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
F1	**PAT** Process Average Testing		Not performed on qualification lots listed on traceability section of this report. To be implemented starting from first production lot		
F2	**SBA** Statistical Bin/Yield Analysis				

Test group G: Cavity Package Integrity Tests					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
G1	**MS** Mechanical Shock	Not applicable: not for plastic packaged devices			
G2	**VFV** Variable Frequency Vibration				
G3	**CA** Constant Acceleration				
G4	**GFL** Gross/Fine Leak				
G5	**DROP** Package Drop				
G6	**LT** Lid Torque				
G7	**DS** Die Shear				
G8	**IWV** Internal Water Vapor				

- 5. Robustness validation activity results (2x AEC-Q100)

After the standard AEC-Q100 duration as reported in section 4 of this report a robustness activity up to 2x AEC-Q100 requirement:

AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
A3	**AC** Autoclave	**ENV. SEQ.** Environmental Sequence **TC** (Ta=-65ºC / +150ºC for 100 cycles) + **AC** (Ta=121ºC, Pa=2atm for 96 hours)	67/6	0/67/6	
A4	**TC** Temp. Cycling	Ta=-65ºC / +150ºC for **1000 cycles**	67/6	0/67/6	

No rejects were detected at final electrical testing as well as no abnormal break loads or forbidden failure modes were detected at the subsequent Wire Bond Pull/Shear tests (WBP, WBS).

VN7016AJTR: Product Optimization

WHAT*:*

Please be informed that in order to rationalize our product portfolio related to VIPower M0-7 family, and following PCN 9126 dated March 2105, New Ordering Code (Commercial Part-numbers) have been introduced.

New part number VN7016AJEPTR will be assembled in dual source PowerSSO-16 assembly line: Bouskoura-Morocco and Shenzhen-China introducing the PSSO-16 Deep Down Set (DDS) lead frame version.

Strip test* will be introduced as well.
Strip test* consists in testing the device directly on the Lead Frame form (strip) before singulating it (2nd crop).
Same test coverage and quality will be applied.

*see below details about strip test

WHY:
Service Improvement, product portfolio optimization

HOW:
See enclosed presentation

WHEN:

Optimized Product version VN7016AJEPTR is already available. We strongly recommend to replace old version with new for a better service

VN7016AJTR vs VN7016AJEPTR
Product Optimization

life.augmented

VN7016AJTR vs VN7016AJEPTR

Optimized version

- New Ordering Code (Commercial Part-number) have been introduced for Optimized Product version:
- Current Ordering Code is now Not Recommended for New Designs (NRND)
- New Ordering Code is the one to be used for qualification and production in any new project
- Current Ordering Code are strongly recommended to be replaced by New Ordering Code in running projects taking advantage of better service.

VN7016AJTR vs VN7016AJEPTR

Optimized version

- New part number will be assembled in dual source PowerSSO-16 assembly line: Bouskoura-Morocco and Shenzhen-China.

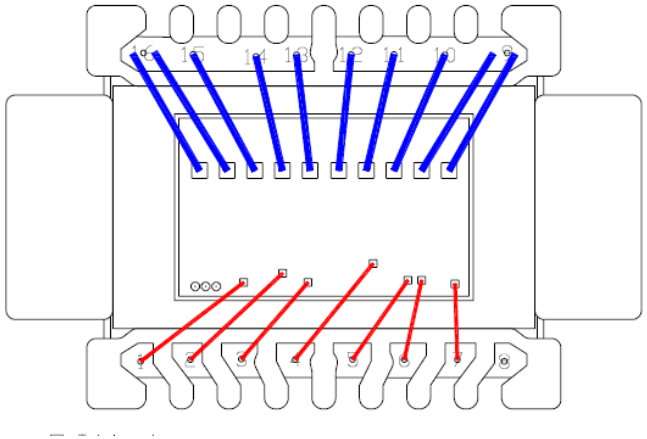
	Current Ordering Code (VN7016AJTR)	New Ordering Code (VN7016AJEPTR)
Silicon	-	No change
Assembly Strategy	ST Bouskoura	PCN 9126 (PSSO-16 Shenzhen second site activation)
Datasheet	No differences (excluded p/n itself and Exposed Pad Dimensions)	
Device Marking	VS7016A	VS7016L
Product status	Qualified and in mass production	
Marketing Status	NRND (Not recommended for new design)	Active

VN7016AJTR vs VN7016AJEPTR

Optimized version

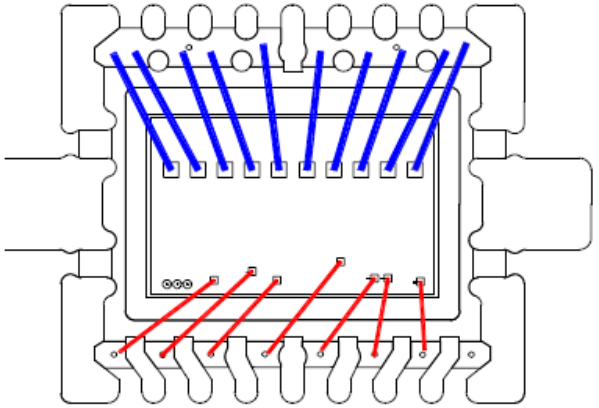
Current Lead Frame Version (ST Bouskoura only)

Pad size: 4.45 x 2.56 mm



New Deep Down Set Lead Frame Version (ST Bouskoura /ST Shenzhen)

Pad size: 3.61 x 2.49 mm



VN7016AJTR vs VN7016AJEPTR

Optimized version

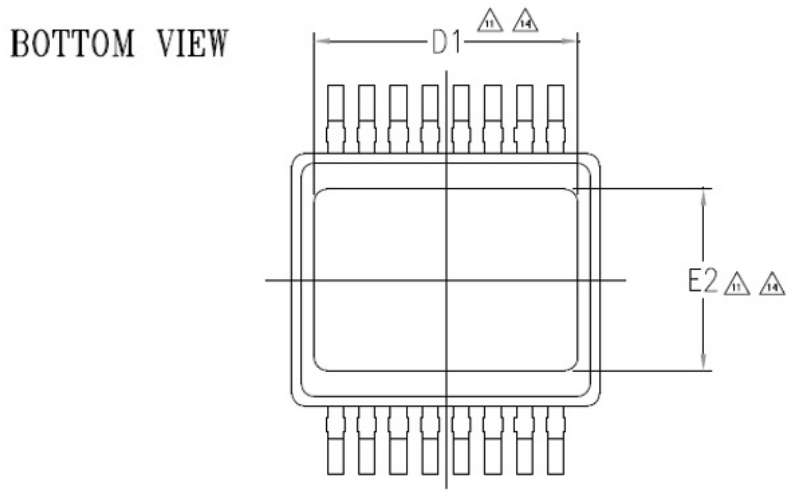
Exposed Pad Dimensions Difference

Current

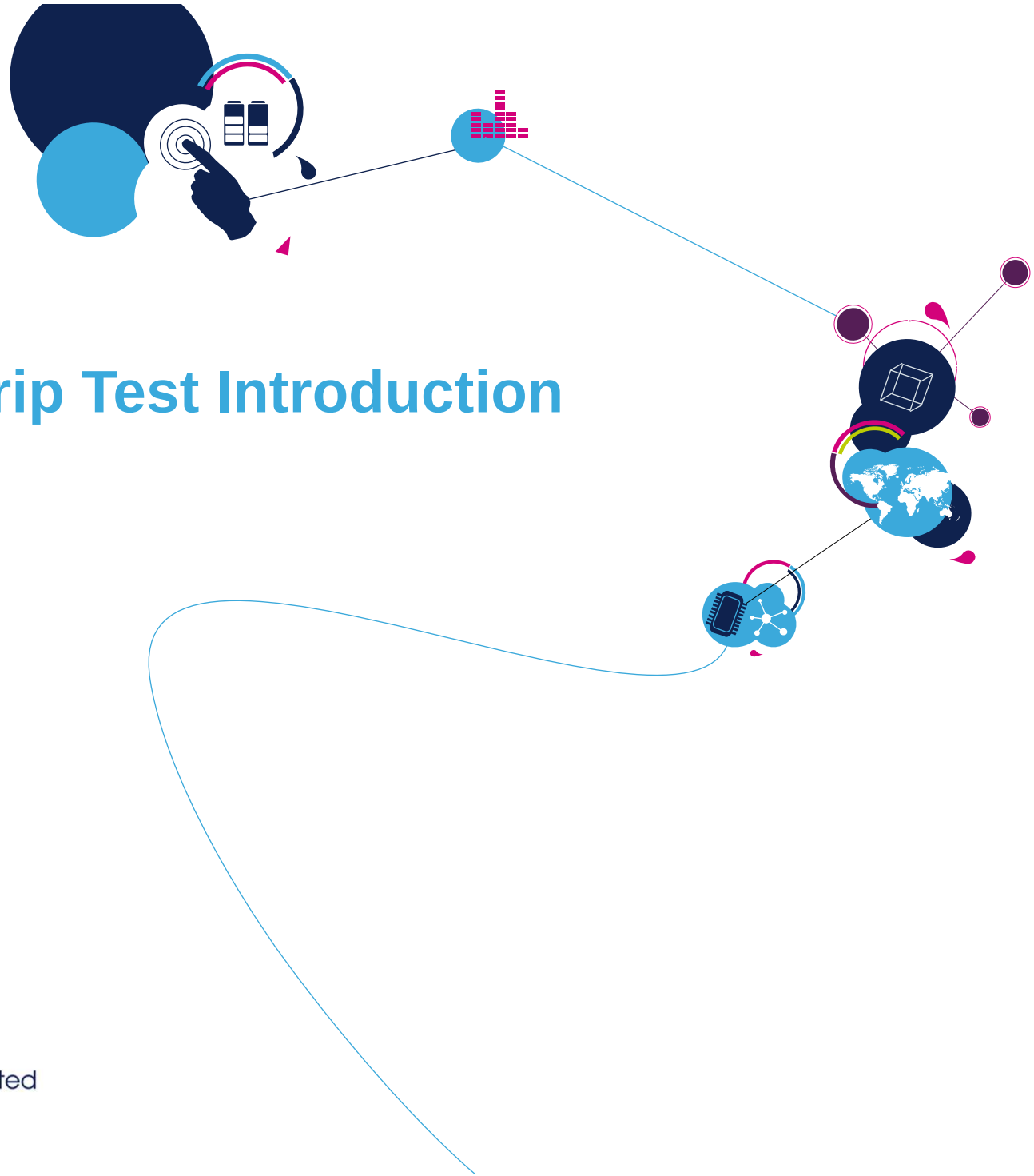
	min	typ	max
D1	2.6		4.2
E2	1.9		2.5

New

	min	typ	max
D1	2.9		3.5
E2	2.2		2.8



life.augmented



PSSOxx: Strip Test Introduction

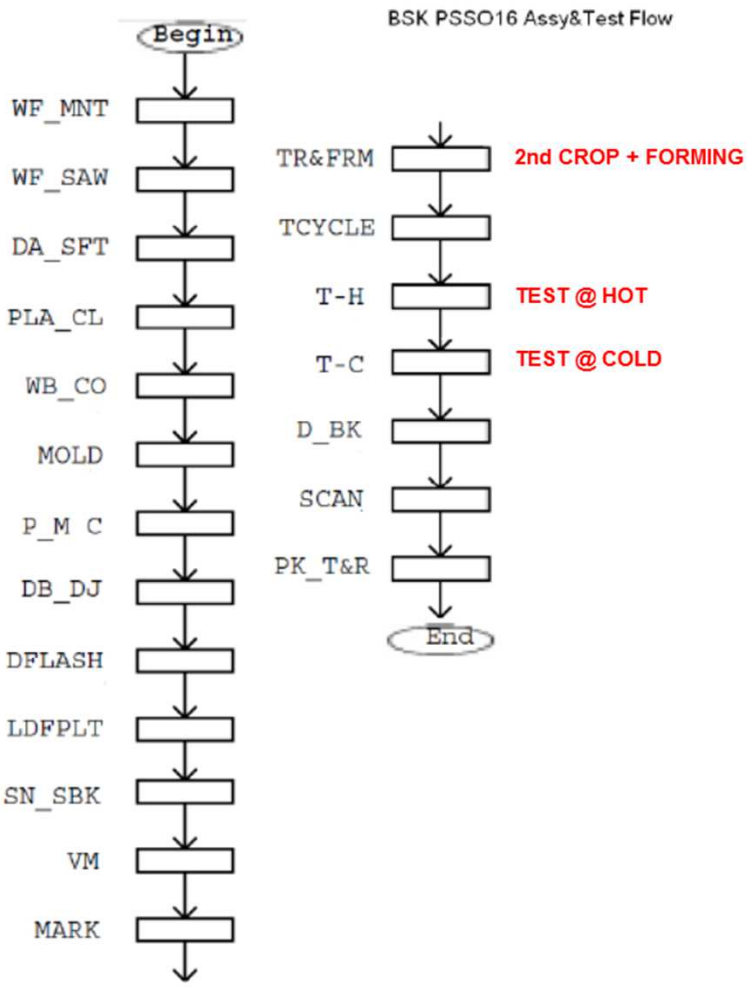
life.augmented

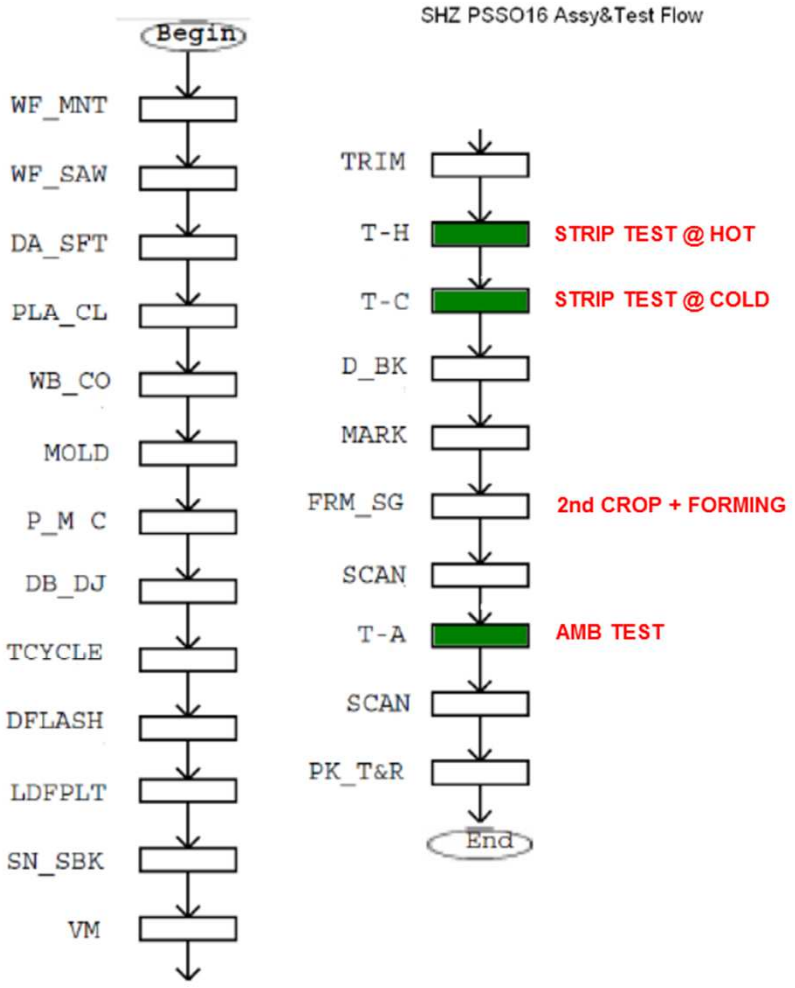
PSSO Strip Test Introduction

- Strip test is a new testing methodology that does not impact fit, form and function nor reliability of the products.
- Materials and equipments are not changed neither at FE nor at BE level
- Strip test is performed in between 1st crop (dam-bar cut) and 2nd crop (Trim&Form and final singulation)
- Further test step at ambient temperature is inserted after vision check

Here follows some slides to explain this new testing methodology.

PSSO OLD vs NEW Flow



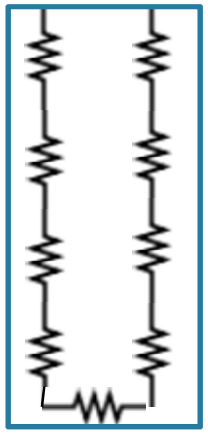


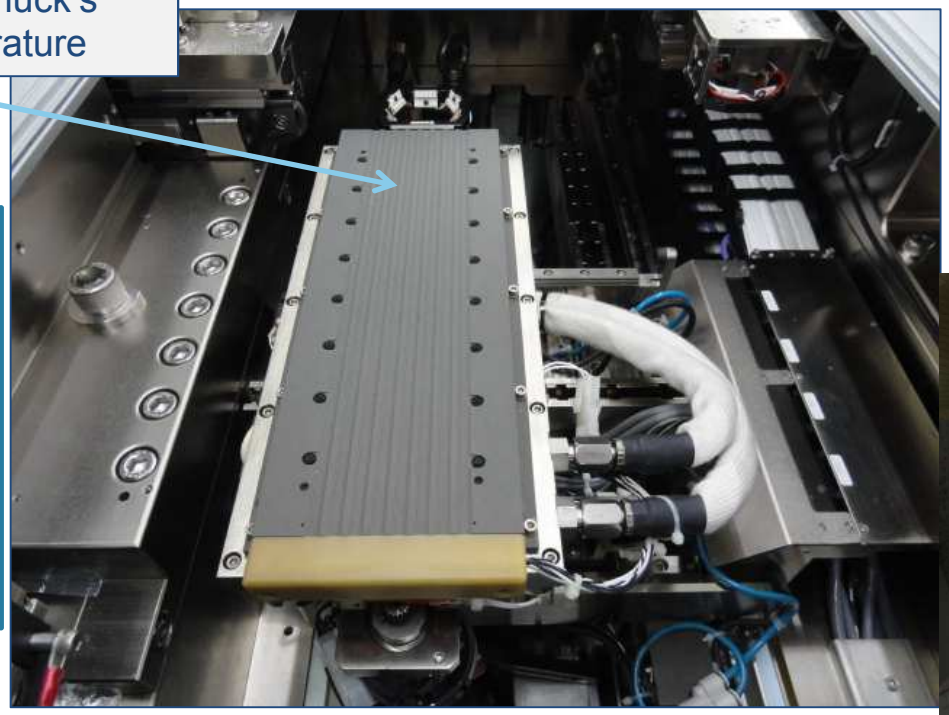
life.augmented

PSSO Strip Test

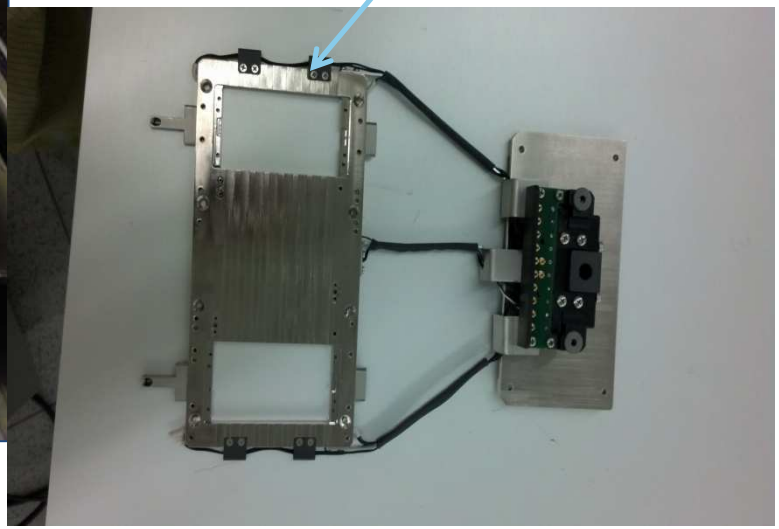
How uniform temperature is ensured?

Resistance used to settle chuck's temperature





Tccf tool used to stabilize frame's temperature



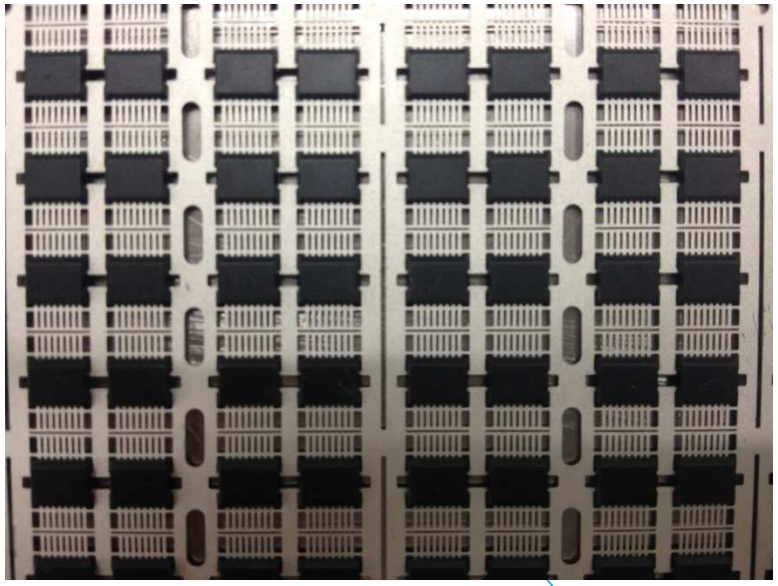
- Same concept used in EWS for the wafer.
- The frame is uniformly heated or cold down and the temperature is stable (T=130degC or T=-40degC)

life.augmented

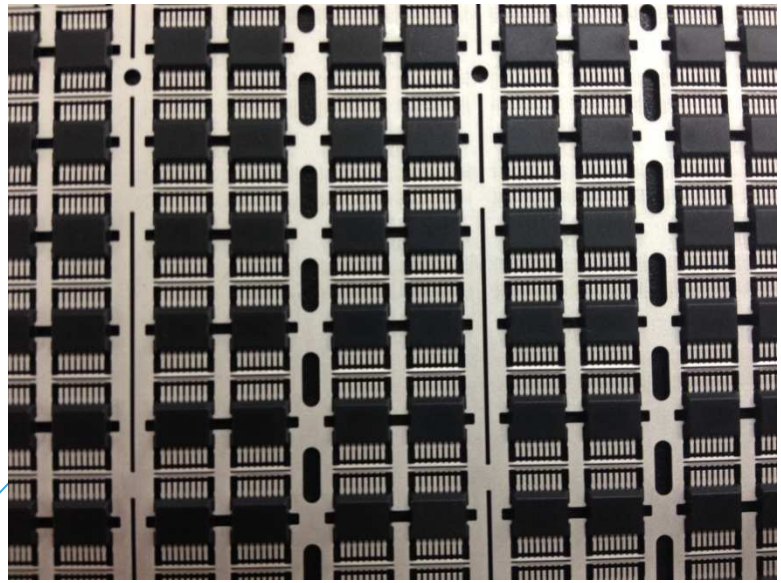
PSSO Strip Test

Leadframe before and after 1st crop

BEFORE 1st CROP



AFTER 1st CROP

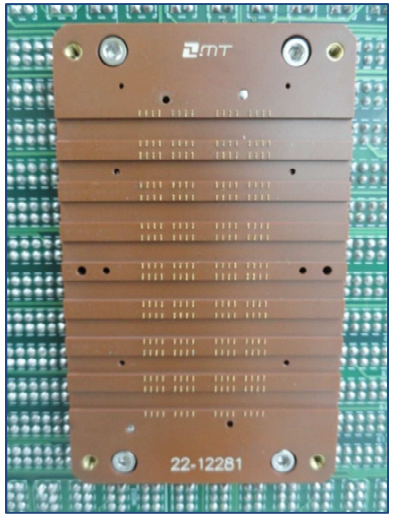


Dam-bar in between leads is cut during the 1st crop
As consequence pins are singulated

PSSO Strip Test

Strip Jig/Contact

Testing Jig



Contact Pogo Pin 32 sites

Test Head + Handler

- Pins are not clamped
- Contact Pogo Pins system is used

life.augmented